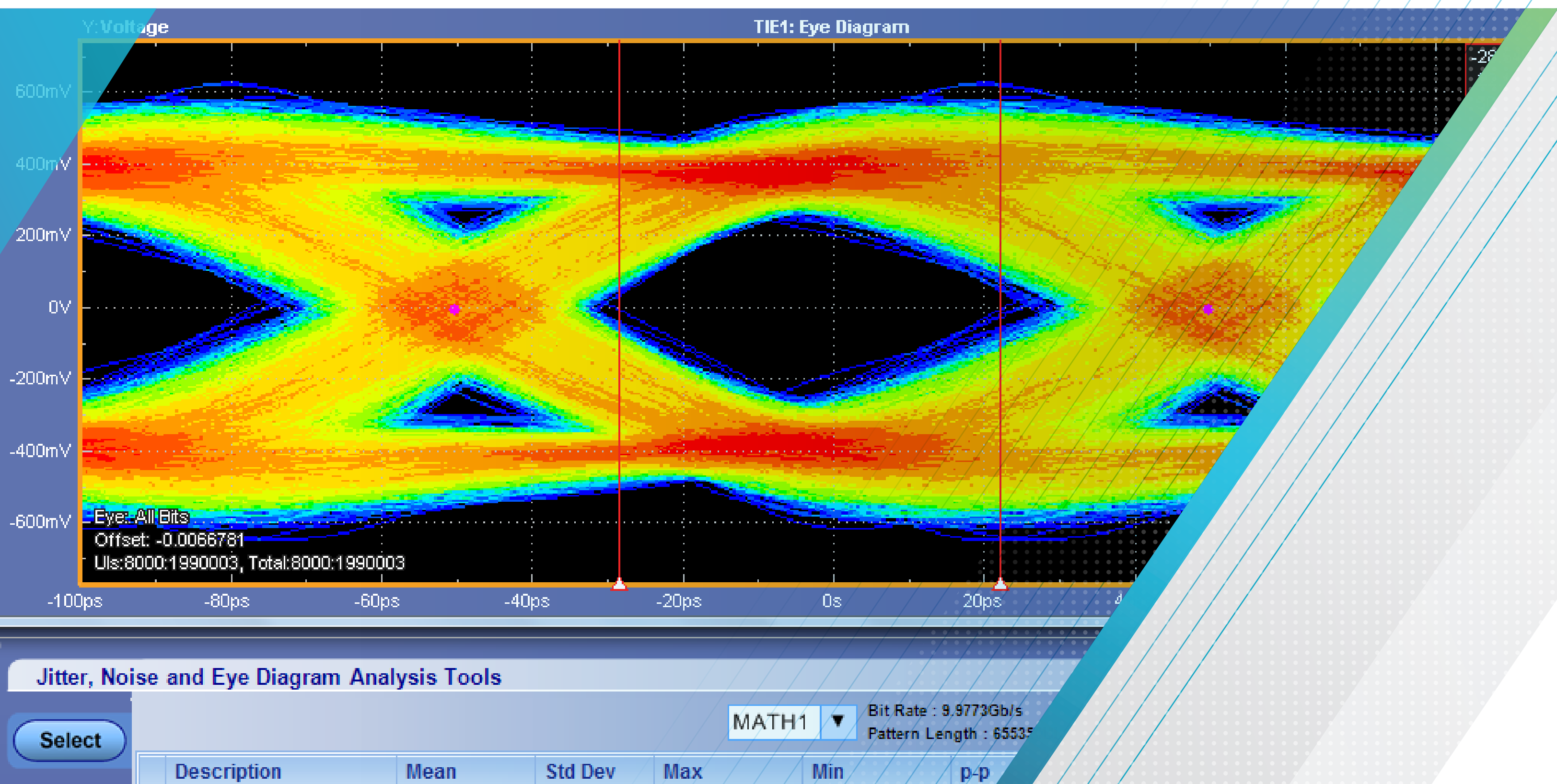
How to Debug USB 3.1 Gen 1 & Gen 2 Electrical Compliance Failures

APPLICATION NOTE



1. Introduction:

The USB Type-C™ connector provides a smaller, thinner and more robust alternative to existing USB 3.1 connectors such as Standard and Micro. With the new Type-C connector the users can plug devices into hosts and hubs in both the directions compared to older connectors which were keyed to plugged in one way only. This reversible feature of the connector greatly simplifies the user experience. The application of the Type-C connector is expected to be adopted by all of the consumer market driven by the needs of ultra-thin consumer devices such as notebooks, tablets, smart phones, etc. where existing Standard-A and Micro-AB receptacles have too large of a form factor to meet those design needs.

Some of the USB 3.1 Type-C specification benefits include faster transfer rate, support for other high speed serial technologies such as Thunderbolt, DisplayPort over a single consolidated Type-C connector, a better mechanical design with a reversible connector. Simplified user experience is one of the reasons USB has been so successful in the peripheral consumer market. Another reason USB has done well is because of the ecosystem built to ensure product interoperability and the USBIF compliance and logo certification program supported by the growing number of test houses.

Tektronix is a major contributor to the USBIF certification program and provides complete automated and debug solution for USB Type-C electrical physical layer testing for Gen1 and Gen2.

2. Measurements supported

Tektronix supports all compliance (Normative) and informative measurements required for compliance certification. Key measurements are Jitter budget, eye diagrams, width@BER, SSC measurements (for SSC enabled DUTs), Tx equalization and LFPS.

The detailed list of normative measurements run is shown below:

Normative Tests	Gen1 (5G)	Gen2 (10G)
Tx Electrical Parameters		
Unit Interval	✓	✓
Random Jitter (Dual-Dirac)	✓	✓
Mask Hits	✓	✓
SSC		
TSSC-Freq-Dev-Max	✓	✓
TSSC-Freq-Dev-Min	✓	✓
TSSC-Mod Rate	✓	✓
SSC_dfdt		✓
Tx Eye Mask		
Deterministic Jitter (Dual-Dirac)	✓	✓
Total Jitter (Dual-Dirac)	@1E-12 BER	@1E-12 BER
Eye Height	✓	✓
Eye Width	@1E-12 BER	@1E-6 BER
TxEQ		
PreShoot		✓
DeEmphasis		✓
LFPS		
Duty Cycle	✓	
Fall Time	✓	
Rise Time	✓	
TPeriod	✓	
Vcm-AC	✓	
Vtx-Diff-PP	✓	
TBurst	✓	
TRepeat	✓	

FIGURE 1. USB 3.1 Tx Normative tests for Gen1/Gen2.

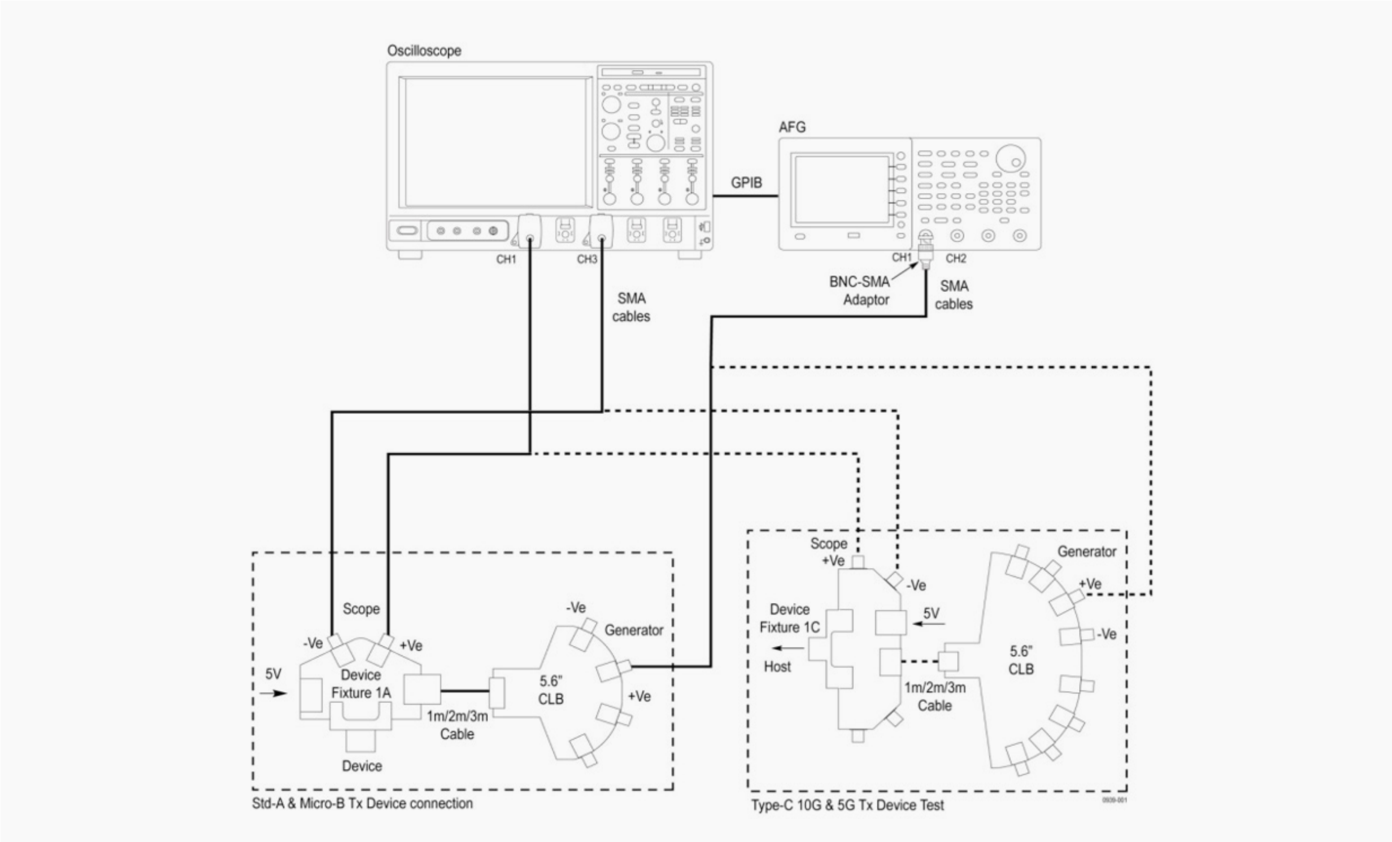


FIGURE 2. Example test setup for USB 3.1 Gen2 Device Transmitter testing.

One example for how to setup for Tx measurements is shown above (USB Device Testing). The schematic shows the possible configurations for both USB 3.1 Standard-A and Type-C.

For USB Type-C, channel loss for Host or Device DUTs are the same unlike for the previous connectors which had different channel loss budget for host and device. Total channel loss for Type-C Gen2 is 23 dB and for Gen1 is 20 dB.

The compliance test point for all measurements is shown below. Measurements are made at the test point (TP1), and Tx specifications are applied after processing the measured data with the compliance reference equalizer.

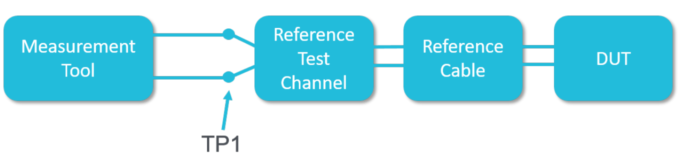


FIGURE 3. Compliance test point reference.

Both short and long channel testing is required to comply with the requirements of the CTS. Short channel testing is performed with a direct connection to the Tx device using simple breakout fixture available from the USB-IF. Long Channel testing is performed by embedding the cable and fixture loss into the data that is captured.

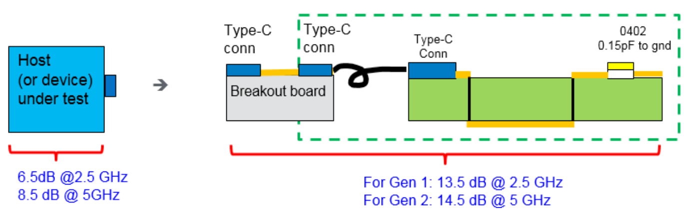


FIGURE 4. Channel budget for USB Type-C.

3. Sigtest and DPOJET

Sigtest is an offline analysis tool for compliance provided by USB-IF. Whereas DPOJET is Tektronix internal tool for compliance and debug testing. Here are the list of measurements which Sigtest and DPOJET support:

USB Type-C Gen1		
Measurements	**Sigtest v3.2.11.3**	**DPOJET**
Jitter budget(RJ,DJ and TJ)	Yes	Yes
Eye diagram	Yes	Yes
Width@BER	Yes	Yes
SSC deviation	No	Yes
SSC modulation rate	No	Yes
Differential pk-pk voltage	No	Yes
LFPS	Yes	Yes
USB Type-C Gen2		
Measurements	**Sigtest v4.0.23.2**	**DPOJET**
Jitter budget(RJ,DJ and TJ)	Yes	Yes
Eye diagram	Yes	Yes
Width@BER	Yes	Yes
Height@BER	No	Yes
SSC deviation	Yes	Yes
SSC modulation rate	Yes	Yes
Differential pk-pk voltage	No	Yes
LFPS	Yes	Yes
Tx Equalization	Yes	Yes

FIGURE 5. Test comparison between SigTest and DPOJET.

4. DPOJET as a Debug Tool

Where TekExpress is purely a compliance-based testing tool, DPOJET is a more comprehensive tool for digging into the causes of compliance test failures and characterization/verification of early designs to determine performance and get early insight to issues that may affect compliance test performance. DPOJET provides detailed control over measurement parameters, and reporting capabilities that allow users to document test outcomes for future reference or sharing with global teams. The following examples show how DPOJET can be used to dig into test failures, and provide confidence in design compliance to the USB specification.

Time Interval Error (TIE) measurements give a view of overall effects that jitter has on a system under test. TIE is a good starting point for determining how much jitter is present in the system, and then more specific jitter measurements such as Random Jitter (Rj) and Deterministic Jitter (Dj) can be used to further pin-point possible causes. The plot below shows a system with TIE that is approximately 50% of one Unit Interval (UI) on a USB3.1 Gen2 signal. This amount of TIE would cause failures of most if not all specified jitter amounts, and width requirements.

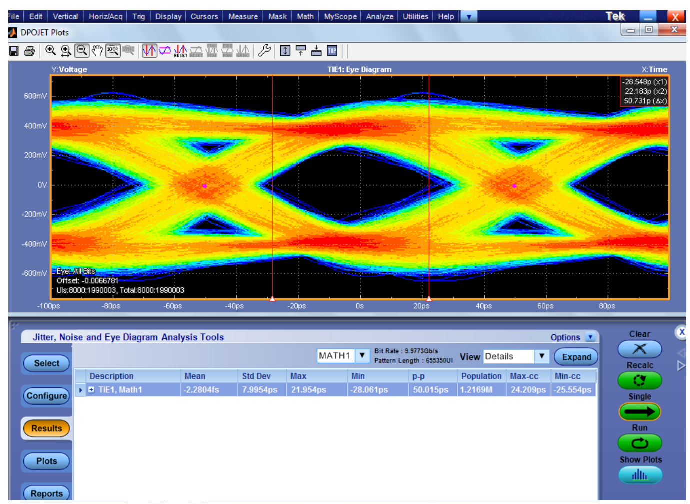


FIGURE 6. High TIE can be cause for test failure, indicating high levels of jitter in DUT.

Eye Diagram analysis using masks is an easy way to determine if a system under test complies with specification requirements at a high level. Mask violations may be related to eye height or eye width requirements, but typically indicate that there could be other problems in the system related to jitter and/or amplitude. Bit errors produced by a system can also be of concern, and can be seen in an eye diagram impinging on the center of the eye. It is good to know that the error is occurring, but DPOJET measurements and plots can take this one step further.

The Mask Hits Eye Diagram plot below shows an eye diagram with a single bit error that has passed through the center of the eye and violated the waveform mask. The Mask Hits Waveform plot on the right gives a bit more information, showing exactly where the errant bit occurred in the waveform, giving users insight into the location of the error and helping them determine exactly when and where the error occurred.

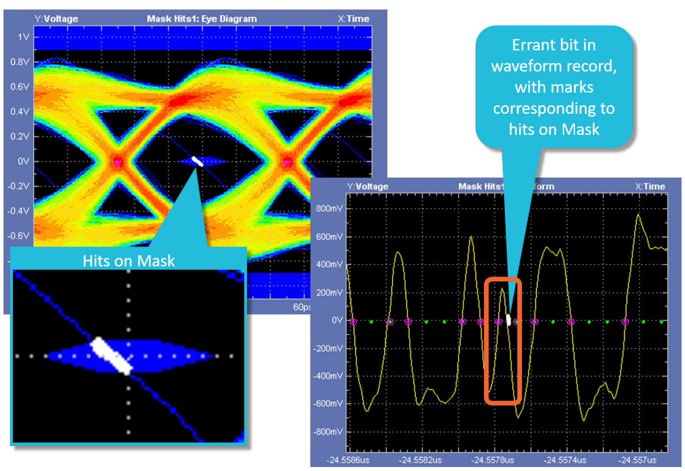


FIGURE 7. Mask hits can be easily located in the waveform record using the Mask Hit Waveform plot in DPOJET.

The following plot details a system that has jitter components beyond what is specified by the USB3.1 specification, which is quickly seen when looking at the eye diagram and further detail is shown in the results panel below the eye. The Total Jitter (Tj) is well-beyond what is acceptable based on current specification guidance.

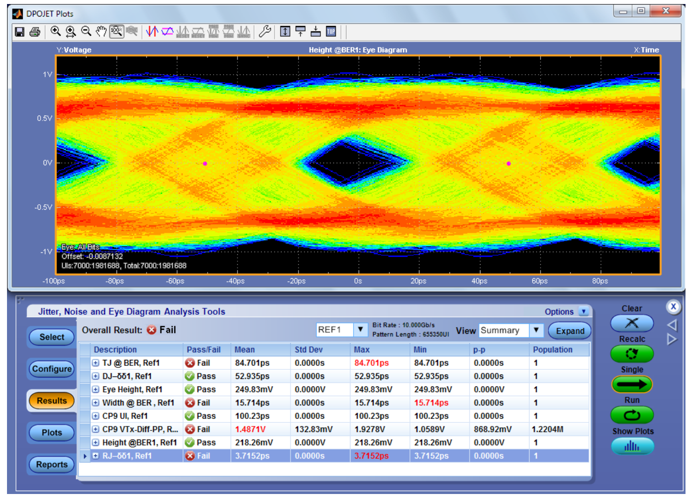


FIGURE 8. High levels of jitter in system cause test failures.

With this last picture of system performance, we get a better sense of possible causes for failures. Though Dj shows as passing, it is extremely close to the limit for failure (53ps). Given that there are many constituent jitter components that comprise the amount of Dj in a system, the causes of Dj are numerous. Dj can be caused by ISI, power supply issues, EMI, impedance mismatches and asymmetry in the system clock, just to name a few. Rj failures are more typically related to thermal noise, and other microscopic effects that are inherent to the physical design of the system.

To build confidence on the margin of devices, you need the ability to render an eye diagram with extrapolation and analyze the channel effect on the signal at the far end using different channel models. Go beyond simple pass/fail compliance and get in-depth debugging insight into compliance failures. DPOJET eye diagram plots with integrated BER contours (shown below) allow users to get an at-a-glance insight into system margin.

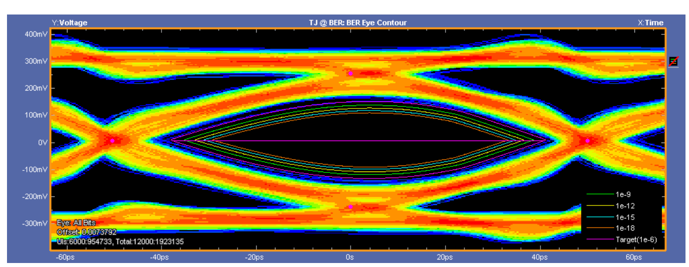


FIGURE 9. The BER Contour plot in DPOJET gives margin confidence with extrapolated contour levels.

5. CTLE with SDLA

For Gen2 testing, all DUTs have to pass through different CTLE parameters to get the maximum eye opening. Using Tektronix SDLA(Serial Data Link Analyzer) and DPOJET, this can be achieved easily.

- USB3.1 specification requires evaluation up to seven combinations of CTLE + DFE and find optimum setting under which to make TX measurements
- TekExpress does 7 presets settings in SDLA automatically.
  - SDLA CTLE equalizer
  - Bit Rate = 10Gb/s Nominal
  - PLL Type = 2
  - JTF BW MHz = 7.5
  - PLL Damp = 0.7
  - Clk Delay ps = 0

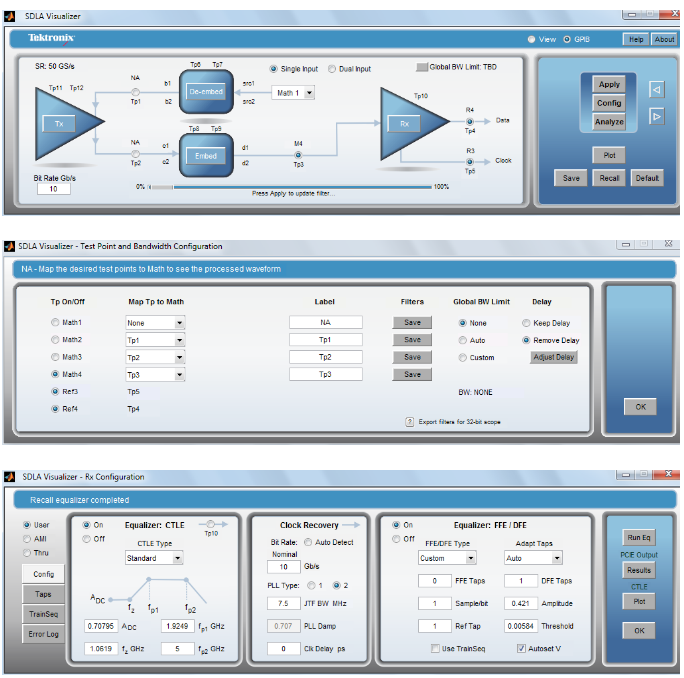


FIGURE 10. SDLA configuration. Find Optimum CTLE + DFE Settings.

The following is what the SDLA tool does for USBSSP:

- Vary CTLE setting, run to auto adjust DFE. Resultant waveform will appear in Ref4.
- Uses its own algorithm to calculate eye height and eye width, record these values
- Once measurements from all Presets are done, multiply eye height value and eye width value, and chooses Preset with largest value
- Perform TX measurements using this Preset.

6. Measurement Reporting

TekExpress and DPOJET reports give detailed information regarding not only measurement results, but a total system snapshot that includes scope settings, SW versions and more. Reports are saved to a single location, along with the waveform data that measurements were taken on, to ensure that the complete picture of system performance can be referenced and even re-created offline. Report archiving enhances confidence and enables a level of collaboration within your global teams to reduce your time to market.

A DPOJET example report has been included in the appendix at the end of this document.

7. Summary

In this application note we've discussed the addition of the Type-C connector and the benefits it brings to USB 3.1. These benefits include a faster transfer rate, support for Thunderbolt, and DisplayPort over a single consolidated Type-C connector, and a better mechanical design with a reversible connector. We've also covered the latest requirements from the USB 3.1 specification, and how Tektronix enables you to go beyond compliance testing with tools designed to help you get to the bottom of issues that can eat into margin and cost valuable testing time.

Tektronix equipment has been, and continues to be used, to certify millions of USB devices through industry workshops and at independent test labs. USB-IF members can leverage the Platform Integration Lab (PIL) to test and correlate early designs. The PIL is available for USB developers to test host and device interoperability and ensure that devices perform correct USB 3.1 electrical and link level signaling.

For more details about USB compliance testing visit the USB Implementers Forum page at www.usb.org. Here you will find detailed test procedures, white papers, and other support materials. Additional information about USB testing can be found at www.tektronix.com/usb. This site includes extensive materials like application notes, webinars and recommended test equipment. The links below will take you to just a few of the documents and webpages available on the Tek.com website to further enhance your understanding of USB testing:

Testing High Speed Serial Standards over Type-C

USB 3.1 What you need to know - Reference Guide

USB 3.1 Receiver Compliance Testing

Simplify your USB Type-C Design Validation - From Complexity to Confidence

8. Appendix

Jitter and Eye Diagram Analysis Tools : Measurement Report

Tektronix
Enabling Innovation

February 26, 2018 11:12:16 AM

Configuration

Setup Configuration

Scope Configuration	
Scope Model	DPO73304DX
Scope Serial No.	PQ00027
Scope Version	10.8.1 Build 37
DPOJET Version	10.0.6.106
SPCStatus	Pass

Probe Configuration				
Probe	Ch1	Ch2	Ch3	Ch4
Name	TCA292D	1X	TCA292D	1X
Serial No.	-	-	-	-
Tip	-	-	-	-
External Attenuation (dB)	0.0	0.0	0.0	0.0
Range	1X	1X	1X	1X
Mode	-	-	-	-

Global Configuration	
Analysis Method	Jitter Only
Jitter Separation Model	Spectral Only
Dual Dirac Model	PCIExpress
Gating	Off
Qualify	Off
Population	Off
Horizontal Display Units	Seconds
Vertical Display Units	Volts
RJ Locked Value	Off

Measurement Configuration

Index	Measurement	Source(s)	Other
1	TJ @ BER (TJ@BER1)	Ref1	Edges => Signal Type: AUTO, Clock Edge: Both | Clock Recovery => Method: PLL – Custom BW, PLL Model: Type II, Damping: 710m, Bandwidth Type: Loop BW, Loop BW: 6MHz, Nominal Data Rate: Manual, Bit Rate: 10Gb/s, Known Data Pattern: Off, Pattern Filename: C:\Users\Public\Tektronix\Tekapplications\DPOJET\Patterns\PRBS127.txt | RjDj => Pattern Detection/Control: Manual, Pattern Type: Arbitrary, Window Length: 9UI, Population: 100, Compensate For Scope Noise:, FalseBER = 1E-6 | Filters => F1: Spec: No Filter, F2: Spec: No Filter | General => Measurement Range Limits: Off, Max: 1ns, Min: 0s, Custom Measurement Name: --
2	DJ–δδ1	Ref1	Edges => Signal Type: AUTO, Clock Edge: Both | Clock Recovery => Method: PLL – Custom BW, PLL Model: Type II, Damping: 710m, Bandwidth Type: Loop BW, Loop BW: 6MHz, Nominal Data Rate: Manual, Bit Rate: 10Gb/s, Known Data Pattern: Off, Pattern Filename: C:\Users\Public\Tektronix\Tekapplications\DPOJET\Patterns\PRBS127.txt | RjDj => Pattern Detection/Control: Manual, Pattern Type: Arbitrary, Window Length: 9UI, Population: 100, Compensate For Scope Noise:, False | Filters => F1: Spec: No Filter, F2: Spec: No Filter | General => Measurement Range Limits: Off, Max: 1ns, Min: 0s, Custom Measurement Name: --
3	Eye Height (Height1)	Ref1	Bit Config => Bit Type: All Bits | Clock Recovery => Method: PLL – Custom BW, PLL Model: Type II, Damping: 710m, Bandwidth Type: Loop BW, Loop BW: 6MHz, Nominal Data Rate: Manual, Bit Rate: 10Gb/s, Known Data Pattern: Off, Pattern Filename: C:\Users\Public\Tektronix\Tekapplications\DPOJET\Patterns\PRBS127.txt | General => Measurement Range Limits: Off, Max: 500mV, Min: 50mV, Custom Measurement Name: --
4	Width @ BER (Width@BER1)	Ref1	Edges => Signal Type: AUTO, Clock Edge: Both | Clock Recovery => Method: PLL – Custom BW, PLL Model: Type II, Damping: 710m, Bandwidth Type: Loop BW, Loop BW: 6MHz, Nominal Data Rate: Manual, Bit Rate: 10Gb/s, Known Data Pattern: Off, Pattern Filename: C:\Users\Public\Tektronix\Tekapplications\DPOJET\Patterns\PRBS127.txt | RjDj => Pattern Detection/Control: Manual, Pattern Type: Arbitrary, Window Length: 9UI, Population: 100, Compensate For Scope Noise:, FalseBER = 1E-6 | Filters => F1: Spec: No Filter, F2: Spec: No Filter | General => Measurement Range Limits: Off, Max: 1us, Min: 1us, Custom Measurement Name: --
5	CP9 UI (SSP UI1)	Ref1	Edges => Signal Type: DATA | Filters => F1: Spec: No Filter, F2: Spec: 3rd Order, Freq: 198kHz, RampTime/F: 5.0505us, BlankingTime/F: 5.0505us | General => Measurement Range Limits: Off, Max: 1ms, Min: 0s, Custom Measurement Name: --
6	CP9 VTx-Diff-PP (SSP VTx-Diff-PP1)	Ref1	Clock Recovery => Method: PLL – Custom BW, PLL Model: Type II, Damping: 710m, Bandwidth Type: Loop BW, Loop BW: 6MHz, Nominal Data Rate: Manual, Bit Rate: 10Gb/s, Known Data Pattern: Off, Pattern Filename: C:\Users\Public\Tektronix\Tekapplications\DPOJET\Patterns\PRBS127.txt | General => Measurement Range Limits: Off, Max: 1V, Min: -1V, Custom Measurement Name: --
7	Height @BER1	Ref1	Bit Config => Bit Type: All Bits, Start: 50%, End: 50%, # of Bins: 1 | Clock Recovery => Method: PLL – Custom BW, PLL Model: Type II, Damping: 710m, Bandwidth Type: Loop BW, Loop BW: 6MHz, Nominal Data Rate: Manual, Bit Rate: 10Gb/s, Known Data Pattern: Off, Pattern Filename: C:\Users\Public\Tektronix\Tekapplications\DPOJET\Patterns\PRBS127.txt | BER => Target BER: 6 | General => Measurement Range Limits: Off, Max: 500mV, Min: 50mV, Custom Measurement Name: --
8	Mask Hits1	Ref1	Bit Config => Bit Type: All Bits, Mask: C:\Users\Public\Tektronix\TekApplications\USBSSP\Masks\USBSSP_Rx_Normative_Short.msk | Clock Recovery => Method: PLL – Custom BW, PLL Model: Type II, Damping: 710m, Bandwidth Type: Loop BW, Loop BW: 6MHz, Nominal Data Rate: Manual, Bit Rate: 10Gb/s, Known Data Pattern: Off, Pattern Filename: C:\Users\Public\Tektronix\Tekapplications\DPOJET\Patterns\PRBS127.txt | General => Measurement Range Limits: Off, Max: 500Hits, Min: 0Hits, Custom Measurement Name: --

Source Reference Levels

Source	Autoset Method	Rise High	Rise Mid	Rise Low	Hysteresis	Fall High	Fall Mid	Fall Low
Ch1	Auto	1V	0V	-1V	30mV	1V	0V	-1V
Ch2	Auto	1V	0V	-1V	30mV	1V	0V	-1V
Ch3	Auto	1V	0V	-1V	30mV	1V	0V	-1V
Ch4	Auto	1V	0V	-1V	30mV	1V	0V	-1V
Math1	Auto	1V	0V	-1V	30mV	1V	0V	-1V
Math2	Auto	182.3mV	-4.1481mV	-190.59mV	13.983mV	182.3mV	-4.1481mV	-190.59mV
Math3	Auto	1V	0V	-1V	30mV	1V	0V	-1V
Math4	Auto	1V	0V	-1V	30mV	1V	0V	-1V
Ref1	Auto(Low-High(full wfm))	402.38mV	-12.793mV	-427.97mV	31.138mV	402.38mV	-12.793mV	-427.97mV
Ref2	Auto	1V	0V	-1V	30mV	1V	0V	-1V
Ref3	Auto(Low-High(full wfm))	199.31mV	-302.01uV	-199.91mV	14.971mV	199.31mV	-302.01uV	-199.91mV
Ref4	Auto((Min-Max))	169.62mV	4.3669mV	-160.89mV	12.394mV	169.62mV	4.3669mV	-160.89mV

Miscellaneous Settings

	Gating	Qualify	Population
State	Off	Off	Off
Source	--	--	--
Size	--	--	--

FIGURE 11A. Example DPOJET Report.

DataRate and Pattern Length

Source	Data Rate	Pattern Type	Pattern Length
REF1	10.000Gb/s	Repeating	655350UI

Measurement Results

Hide Current Aquisitions | Summary View

Description	Mean	Std Dev	Max	Min	High Limit	Low Limit	High Margin	Low Margin	p-p	Population	Max-cc	Min-cc	Pass/Fail
TJ @ BER, Ref1	37.659ps	0.0000s	37.659ps	37.659ps	Max : 67.100ps		Max : 29.441ps		0.0000s	1	0.0000s	0.0000s	Pass
Current Acquisition	37.659ps	0.0000s	37.659ps	37.659ps	--	--	--	--	0.0000s	1	0.0000s	0.0000s	--
DJ–δδ1, Ref1	5.9603ps	0.0000s	5.9603ps	5.9603ps	Max : 53.000ps		Max : 47.040ps		0.0000s	1	0.0000s	0.0000s	Pass
Current Acquisition	5.9603ps	0.0000s	5.9603ps	5.9603ps	--	--	--	--	0.0000s	1	0.0000s	0.0000s	--
Eye Height, Ref1	269.82mV	0.0000V	269.82mV	269.82mV	Min : 1.2000V	Min : 70.000mV	Min : 930.18mV	Min : 199.82mV	0.0000V	1	0.0000V	0.0000V	Pass
Current Acquisition	269.82mV	0.0000V	269.82mV	269.82mV	--	--	--	--	0.0000V	1	0.0000V	0.0000V	--
Width @ BER , Ref1	62.502ps	0.0000s	62.502ps	62.502ps		Min : 48.000ps		Min : 14.502ps	0.0000s	1	0.0000s	0.0000s	Pass
Current Acquisition	62.502ps	0.0000s	62.502ps	62.502ps	--	--	--	--	0.0000s	1	0.0000s	0.0000s	--
CP9 UI, Ref1	100.23ps	0.0000s	100.23ps	100.23ps	Mean : 100.53ps	Mean : 99.970ps	Mean : 296.47fs	Mean : 263.53fs	0.0000s	1	0.0000s	0.0000s	Pass
Current Acquisition	100.23ps	0.0000s	100.23ps	100.23ps	--	--	--	--	0.0000s	1	0.0000s	0.0000s	--
CP9 VTx-Diff-PP, Ref1	1.2217V	109.85mV	1.5963V	744.64mV	Mean : 1.2000V	Mean : 70.000mV	Mean : -21.722mV	Mean : 1.1517V	851.68mV	1.2203M	395.76mV	-404.00mV	Fail
Current Acquisition	1.2217V	109.85mV	1.5963V	744.64mV	--	--	--	--	851.68mV	1.2203M	395.76mV	-404.00mV	--
Height @BER1, Ref1	429.31mV	0.0000V	429.31mV	429.31mV	Min : 1.2000V	Min : 70.000mV	Min : 770.69mV	Min : 359.31mV	0.0000V	1	0.0000V	0.0000V	Pass
Current Acquisition	429.31mV	0.0000V	429.31mV	429.31mV	--	--	--	--	0.0000V	1	0.0000V	0.0000V	--
Mask Hits1, Ref1	1.0000		1.0000	1.0000	Max : 1					7000			Fail
Hits In Segment 1	0.0000		0.0000	0.0000	--	--	--	--		7000			--
Hits In Segment 2	1.0000		1.0000	1.0000	--	--	--	--		7000			--
Hits In Segment 3	0.0000		0.0000	0.0000	--	--	--	--		7000			--

Pass/Fail Summary

Limits Information

Location C:\Users\Public\Tektronix\TekApplications\USBSSP\Limits
File Name USBSSP_CP9_Normative_Limits.xml
Description

Pass/Fail Information

Measurement	TJ @ BER			
Source1	Ref1			
	Value	High Limit	Low Limit	Pass Fail
Max	37.659ps	67.100ps		Pass

Pass/Fail Information

Measurement	DJ–δδ1			
Source1	Ref1			
	Value	High Limit	Low Limit	Pass Fail
Max	5.9603ps	53.000ps		Pass

Pass/Fail Information

Measurement	Eye Height			
Source1	Ref1			
	Value	High Limit	Low Limit	Pass Fail
Min	269.82mV	1.2000V	70.000mV	Pass

Pass/Fail Information

Measurement	Width @ BER			
Source1	Ref1			
	Value	High Limit	Low Limit	Pass Fail
Min	62.502ps		48.000ps	Pass

Pass/Fail Information

Measurement	CP9 UI			
Source1	Ref1			
	Value	High Limit	Low Limit	Pass Fail
Mean	100.23ps	100.53ps	99.970ps	Pass

Pass/Fail Information

Measurement	CP9 VTx-Diff-PP			
Source1	Ref1			
	Value	High Limit	Low Limit	Pass Fail
Mean	1.2217V	1.2000V	70.000mV	Fail

Pass/Fail Information

Measurement	Height @BER1			
Source1	Ref1			
	Value	High Limit	Low Limit	Pass Fail
Min	429.31mV	1.2000V	70.000mV	Pass

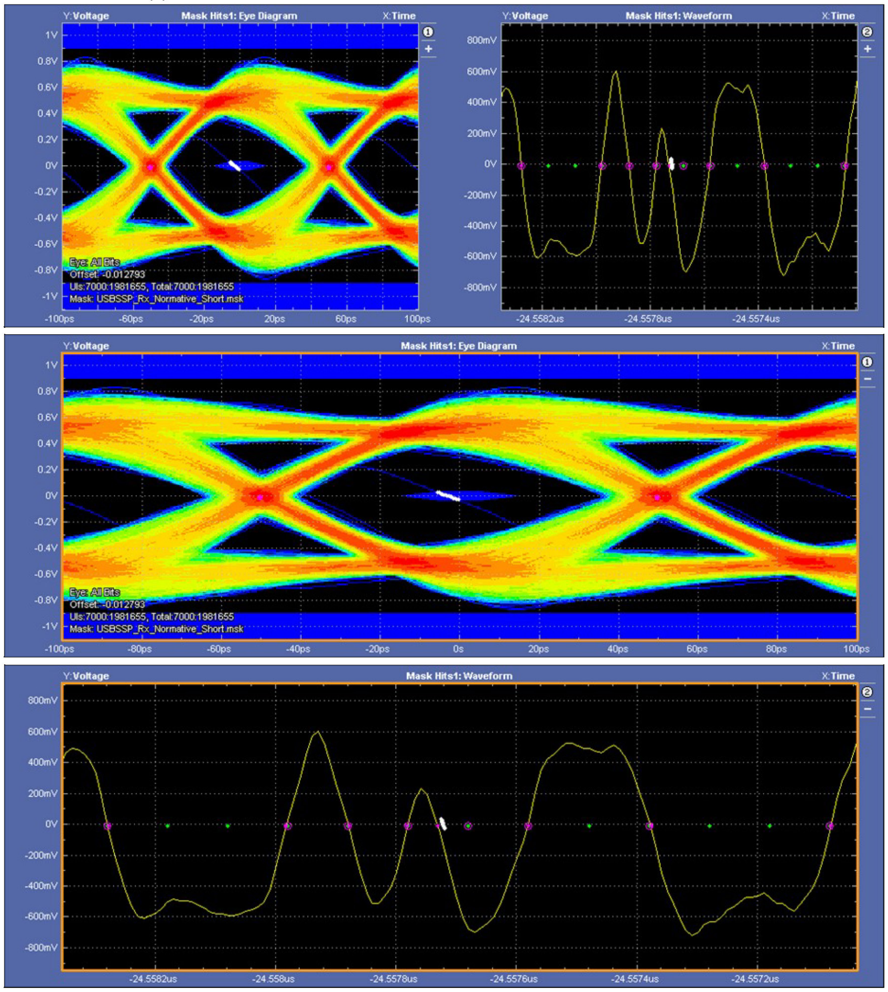
Pass/Fail Information

Measurement	Mask Hits1
Source1	Ref1

FIGURE 11B. Example DPOJET Report.

	Value	High Limit	Low Limit	Pass Fail
Max	1.0000	1		Fail

- Plot Images
  - Measurement Plot(s)



- Oscilloscope Waveform

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FIGURE 11C. Example DPOJET Report.

Contact Information:

Australia* 1 800 709 465
Austria 00800 2255 4835
Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777
Belgium* 00800 2255 4835
Brazil +55 (11) 3759 7627
Canada 1 800 833 9200
Central East Europe / Baltics +41 52 675 3777
Central Europe / Greece +41 52 675 3777
Denmark +45 80 88 1401
Finland +41 52 675 3777
France* 00800 2255 4835
Germany* 00800 2255 4835
Hong Kong 400 820 5835
India 000 800 650 1835
Indonesia 007 803 601 5249
Italy 00800 2255 4835
Japan 81 (3) 6714 3086
Luxembourg +41 52 675 3777
Malaysia 1 800 22 55835
Mexico, Central/South America and Caribbean 52 (55) 56 04 50 90
Middle East, Asia, and North Africa +41 52 675 3777
The Netherlands* 00800 2255 4835
New Zealand 0800 800 238
Norway 800 16098
People's Republic of China 400 820 5835
Philippines 1 800 1601 0077
Poland +41 52 675 3777
Portugal 80 08 12370
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